Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (Currently amended): A caching system, comprising:

a tail FIFO ~~memory~~ having a tail input to receive incoming data and a tail output to output the incoming data;

a memory having a memory input and a memory output, the memory input is coupled to the tail output and the memory is operable to store the incoming data that is output from the tail output, and wherein the memory is operable to output the stored data at the memory output;

a multiplexer having first and second multiplexer inputs coupled to the tail output and the memory output, respectively, the multiplexer having a control input to select one of the multiplexer inputs to ~~coupled~~ couple to a multiplexer output;

a head FIFO ~~memory~~ having a head input coupled to the multiplexer output to receive the incoming data, and a head output to output the incoming data; and

a controller coupled to the tail FIFO, the head FIFO, and the memory and operable to transfer one or more blocks of the incoming data having a selected block size from the tail FIFO to the memory and from the memory to the head FIFO, wherein the selected block size provides a selected memory transfer efficiency level.

Claim 2 (Original): The system of claim 1, wherein the head FIFO further comprises a head fill indicator coupled to the controller to indicate a fill characteristic of the head FIFO.

Claim 3 (Original): The system of claim 2, wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the tail FIFO to the memory based on the head fill indicator.

Claim 4 (Original): The system of claim 2, wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the memory to the head FIFO based on the head fill indicator.

Claim 5 (Original): The system of claim 1, wherein the tail FIFO further comprises a tail fill indicator coupled to the controller to indicate a fill characteristic of the tail FIFO.

Claim 6 (Original): The system of claim 5, wherein the controller transfers the one or more blocks of the incoming data having the selected block size from the tail FIFO to the memory based on the tail fill indicator.

Claim 7 (Original): The system of claim 1, wherein the incoming data comprises data frames of varying length and where the one or more blocks are defined to include data from one or more of the data frames, and wherein a selected block may contain data from two or more data frames.

Claim 8 (Original): The system of claim 1, wherein the controller includes a control output coupled to the control input of the multiplexer, wherein the controller is operable to control which of the multiplexer inputs is coupled to the multiplexer output.

Claim 9 (Original): The system of claim 1, wherein a data path to the memory is wider than a width characteristic of the tail FIFO.

Claim 10 (Currently amended): A method for implementing a caching system, the method comprising steps of:

receiving data at a tail FIFO ~~memory;~~

selecting an efficiency level for operating a memory interface;

determining a selected block size to support the efficiency level;

transferring one or more blocks of the data having the selected block size from the tail FIFO ~~memory~~ to a head FIFO ~~memory~~ when the head FIFO is within a first fill level, wherein the head FIFO ~~memory~~ includes an output to output the data;

transferring the one or more blocks of the data having the selected block size, from the tail FIFO to a memory via the memory interface, when the head FIFO is within a second fill level;

transferring the one or more blocks of data from the memory to the head FIFO when the head FIFO is within a third fill level.

Claim 11 (Original): The method of claim 10, wherein the data comprises data frames of varying length, and the method further comprises a step of defining the one or more blocks of data having the selected block size to include data from one or more of the data frames, and wherein a selected block of data may include data from two or more data frames.

Claim 12 (New): A caching system comprising:

a tail FIFO having

a tail input to receive incoming data

a tail output to output data

a memory having a memory input and a memory output, the memory operable to

store data that is output from the tail output

output data at a memory output

a multiplexer having first and second multiplexer inputs coupled to the tail output and the memory output, respectively, the multiplexer having a control input to select one of the multiplexer inputs to couple to a multiplexer output

a head FIFO having

a head input coupled to the multiplexer output to receive data

a head output to output data, the output data comprising data frames of variable length

a controller

coupled to at least one of the tail FIFO and the head FIFO

coupled to the memory

operable to control transfers of data between the memory and the at least one of the tail FIFO and the head FIFO at a selected efficiency.

Claim 13 (New): The caching system of claim 12 wherein

the incoming data and the output data comprise data frames of variable length

the memory stores data in blocks of at least one fixed size

the controller is to select a block size for the transfer which provides a selected efficiency for the transfers.

Claim 14 (New): The caching system of claim 12 wherein the controller is further operable to control memory transfers from the tail FIFO to the memory in fixed-length blocks, wherein the selected efficiency is achieved at least in part by maximizing an amount of data taken from the tail FIFO and put in the blocks.

Claim 15 (New): The caching system of claim 12 wherein the controller is further operable to control transfers of data from the memory to the head FIFO in fixed-length blocks, wherein the selected efficiency is achieved at least in part by maximizing an amount of data destined for the head FIFO in the blocks.